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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/450,299	04/18/2012	Akira Goda	303.D66US1	9946

73115 7590 04/26/2017

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GONDARENKO, NATALIA A

ART UNIT	PAPER NUMBER
2891	

NOTIFICATION DATE	DELIVERY MODE
04/26/2017	ELECTRONIC

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte AKIRA GODA and ROGER W. LINDSAY

Appeal 2016-001152
Application 13/450,299
Technology Center 2800

Before ADRIENE LEPIANE HANLON, TERRY J. OWENS, and MONTÉ T. SQUIRE, *Administrative Patent Judges*.

OWENS, *Administrative Patent Judge.*

DECISION ON APPEAL

STATEMENT OF THE CASE

The Appellants appeal under 35 U.S.C. § 134(a) from the Examiner's rejection of claims 11, 13–22 and 25–31. We have jurisdiction under 35 U.S.C. § 6(b).

The Invention

The Appellants claim a method which, the Appellants state (Spec. ¶ 8), can form a memory device. Claim 11 is illustrative:

> 11. A method, comprising:
>
> forming a first deck having a number of first levels of conductor material and a number of first levels of dielectric material over a substrate, each level of the number of first levels of conductor material being separated from an adjacent level of conductor material by at least one of the number of first levels of dielectric material;

forming a first set of openings through the number of first levels of conductor material and the number of first levels of dielectric material;

forming a sacrificial material in the first set of openings, the sacrificial material at least partially filling the first set of openings;

forming a second deck over the first deck, the second deck having a number of second levels of conductor material and a number of second levels of dielectric material, each level of the number of second levels of conductor material being separated from an adjacent level of conductor material by at least one of the number of second levels of dielectric material;

forming a second set of openings through the number of second levels of conductor material and the number of second levels of dielectric material, each of the second set of openings being substantially vertically aligned with respective ones of the first set of openings, the second set of openings not having a sacrificial material formed therein at any temporal point during formation of either the first deck or the second deck, the second deck comprising memory devices;

removing the sacrificial material from the first set of openings, forming multi-deck openings through the first deck and the second deck; and

forming silicide substantially concurrently on exposed areas of the first levels of conductor material and the second levels of conductor material within at least some of the multi-deck openings.

The References

Sakaguchi	US 2009/0230449 A1	Sep. 17, 2009
Son (Son '966)	US 2009/0242966 A1	Oct. 1, 2009
Kidoh	US 2010/0109072 A1	May 6, 2010
Omura	US 2010/0176440 A1	July 15, 2010
Son (Son '205)	US 2010/0240205 A1	Sep. 23, 2010
Hwang	US 2011/0151667 A1	June 23, 2011
Mizushima	US 2011/0233646 A1	Sep. 29, 2011
Purayath	US 2011/0309430 A1	Dec. 22, 2011

The Rejections

The claims stand rejected under 35 U.S.C. § 103 as follows:

1) claim 11 over Hwang in view of Kidoh and Son '966,
2) claims 11 and 13–15 over Omura in view of Hwang, Kidoh and Son '966,
3) claims 11, 13 and 14 over Kidoh in view of Mizushima and Son '966,
4) claims 16 and 17 over Omura in view of Hwang, Kidoh, Son '966 and Son '205,
5) claims 18–21 over Omura in view of Mizushima, Son '205, Son '966 and Kidoh,
6) claims 18–21 and 30 over Kidoh in view of Son '205 and Son '966,
7) claim 22 over Kidoh in view of Son '205, Son '966 and Sakaguchi,
8) claim 22 over Omura in view of Mizushima, Son '205, Son '966 and Sakaguchi,
9) claims 25–27 over Omura in view of Mizushima, Son '966 and Kidoh,
10) claim 28 over Omura in view of Mizushima, Son '966 and Son '205,
11) claim 29 over Hwang in view of Purayath,
12) claim 30 over Omura in view of Mizushima, Son '205, Son '966 and Kidoh, and
13) claim 31 over Kidoh in view of Purayath, Mizushima and Son '205.

OPINION

We reverse rejections 1, 3, 6, 7, 11 and 13 and affirm rejections 2, 4, 5, 8–10 and 12.

Rejections 1 and 3

We need address only the sole independent claim in rejections 1 and 3, i.e., claim 11. That claim requires forming a first set of openings through a first deck's levels of conductor material, forming a sacrificial

material in the first set of openings, and forming a second set of openings through a second deck's levels of conductor material such that the second set of openings does not have a sacrificial material formed therein at any temporal point during formation of either the first deck or the second deck. To meet that claim requirement the Examiner relies upon Kidoh's paragraph 12 which describes an aspect of the invention without mentioning a sacrificial material in the openings of a second deck (stacked body ML2; Fig. 8A) (Final Act. 4, 13).

Kidoh discloses, with respect to a first embodiment, that openings in a second deck (ML2) are filled with a sacrificial member (53) (¶¶ 52, 58; Fig. 9A), and Kidoh describes the other embodiments as differing from the first embodiment in ways unrelated to the sacrificial member (¶¶ 72, 75, 76, 78, 81, 82–86, 88, 90). Thus, the Examiner's finding that Kidoh forms second deck openings not having a sacrificial material therein at any temporal point during formation of the first or second deck is not supported by Kidoh's disclosure.

The Appellants' claim 11 also requires "forming silicide substantially concurrently on exposed areas of the first levels of conductor material and the second levels of conductor material within at least some of the multi-deck openings."

Son '966 discloses a nonvolatile memory device wherein, in a gap between insulation interlayer patterns (104), a low resistance metal silicide pattern (162) word line contacts a control gate pattern (131a)'s surface such that the operating speed of the device may be increased (¶¶ 215, 221; Fig. 33).

The Examiner concludes that Son '966 would have suggested forming metal silicide substantially concurrently on Kidoh's first deck's and second deck's levels of conductor material to increase the device's operating speed (Final Act. 14; Ans. 5).

"A rejection based on section 103 clearly must rest on a factual basis, and these facts must be interpreted without hindsight reconstruction of the invention from the prior art." *In re Warner*, 379 F.2d 1011, 1017 (CCPA 1967).

The increased operating speed benefit relied upon by the Examiner is a characteristic of Son '966's device. The Examiner does not address the differences between Kidoh's and Son '966's devices and establish that, regardless of those differences, one of ordinary skill in the art would have been motivated to modify Kidoh's device as proposed by the Examiner and would have had a reasonable expectation that the modified device would have the relied-upon beneficial characteristic of Son '966's device. *See In re Vaeck*, 947 F.2d 488, 493 (Fed. Cir. 1991); *In re O'Farrell*, 853 F.2d 894, 902 (Fed. Cir. 1988).

Rejections 6 and 7

We need address only the sole independent claim in rejections 6 and 7, i.e., claim 18. That claim requires substantially concurrently removing a portion of a first charge-storing material and a second charge-storing material so as to be substantially coplanar with sidewalls of a multi-deck channel opening to form a number of discrete charge storage structures in first and second decks. To meet that claim requirement the Examiner relies upon Son '205 (Final Act. 24–25).

Son '205 forms a nonvolatile memory device by a method comprising forming openings (134) through a stack of alternating insulating layers (110) and conductive layers (LSL, WL, USL) by removing a portion of a buried conductive layer (151) and a first insulating layer (141), oxidizing the buried conductive layer (151)'s exposed surface to form floating gates (FGs) comprising buried conductive patterns (152), and then forming semiconductor pillars (PL) in the openings (134) (¶¶ 50, 80–85; Figs. 4, 14–16).

The Examiner concludes that it would have been obvious to one of ordinary skill in the art to modify Kidoh's device by "substantially concurrently removing a portion of the first charge-storage material and the second charge-storage material so as to be substantially co-planar with sidewalls of the multi-deck channel opening to form a number of discrete charge storage structures in the first and second decks in order to provide a nonvolatile memory device comprising floating gates interposed between sides of the semiconductor pillars and the word lines, and thus, to obtain [a] three-dimensional device having excellent reliability (Son ('205), ¶0005, ¶0050)" (Final Act. 25).

The excellent reliability benefit relied upon by the Examiner is a characteristic of Son '205's device. The Examiner does not address the differences between Kidoh's and Son '205's devices and establish that, regardless of those differences, one of ordinary skill in the art would have been motivated to modify Kidoh's device as proposed by the Examiner and would have had a reasonable expectation that the modified device would

have the relied-upon beneficial characteristic of Son '205's device. *See Vaeck*, 947 F.2d at 493; *O'Farrell*, 853 F.2d at 902.[1]

Rejections 11 and 13

The Appellants' claims 29 and 31 require forming a sacrificial material fully within a first gate-slit opening, the sacrificial material partially filling the first gate-slit opening and being formed over an air gap located proximal to a substrate and within the first gate-slit opening.

Hwang makes a nonvolatile memory device by a method comprising forming lower deck (100) sacrificial patterns (165) which are removed to form a trench (320) (¶¶ 155, 156, 161–164; Figs. 14–17).

Purayath makes a nonvolatile memory device by a method comprising applying a capping layer (484) over and between stacks such that word line air gaps (486) are formed between the stacks (¶¶ 66–67; Figs. 7O). The air gaps provide electrical isolation or shielding between adjacent stacks (¶ 66).

The Examiner concludes that it would have been obvious to one of ordinary skill in the art to form Hwang's sacrificial material (165) over an air gap "to provide electrical isolation or shielding between elements of adjacent layer stack rows, and thus to provide high density semiconductor device, such as non-volatile storage (Purayath, ¶0003, ¶0066)" (Final Act. 39).

The Examiner does not establish that one of ordinary skill in the art would have considered Purayath's disclosed benefit of the word line air

[1] Also, as with claim 11's silicide-forming step, the Examiner does not establish that Son '966 would have provided one of ordinary skill in the art with an apparent reason to modify Kidoh's method such that it includes that step in claim 18's method.

gaps, i.e., electrical isolation or shielding between adjacent layer stack rows (¶ 66), to be applicable to Hwang's sacrificial layer (165) which is removed during formation of the device (¶ 163). The Examiner, therefore, has not set forth a factual basis which is sufficient to support a prima facie case of obviousness of the methods claimed in the Appellants' claims 29 and 31. *See Warner*, 379 F.2d at 1017.

For the above reasons we reverse rejections 1, 3, 6, 7, 11 and 13.

Rejections 2, 4, 5, 8–10 and 12

The Appellants state that "[a]lthough the undersigned does not admit that *Omura* or *Mizushima* teach or suggest any of the claim elements, the undersigned will instead focus on the misapplication of the cited references to *Hwang*, *Kidoh*, and *Son 1* [i.e., Son '966]" (Br. 21). The Appellants do not challenge rejections 2, 4, 5, 8–10 and 12. Accordingly, we summarily affirm those rejections.

DECISION/ORDER

Rejections 1, 3, 6, 7, 11 and 13 are reversed and rejections 2, 4, 5, 8–10 and 12 are affirmed.

It is ordered that the Examiner's decision is affirmed-in-part.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED-IN-PART